

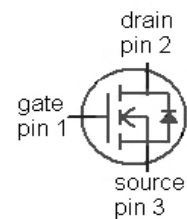
**OptiMOS<sup>®</sup> -T Power-Transistor**

**Product Summary**

$V_{DS}$	55	V
$R_{DS(on),max}$	6.9	m $\Omega$
$I_D$	50	A

**Features**

- N-channel - Normal Level - Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green package (RoHS compliant)
- Ultra low Rds(on)
- 100% Avalanche tested

**PG-TO252-3-11**


Type	Package	Marking
IPD50N06S3-07	PG-TO252-3-11	PN0607

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current <sup>1)</sup>	$I_D$	$T_C=25\text{ °C}$ , $V_{GS}=10\text{ V}$	50	A
		$T_C=100\text{ °C}$ , $V_{GS}=10\text{ V}^{2)}$	50	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	200	
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	$I_D=25\text{ A}$ ,	710	mJ
Avalanche current, single pulse	$I_{AS}$		50	A
Gate source voltage <sup>3)</sup>	$V_{GS}$		$\pm 20$	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	136	W
Operating and storage temperature	$T_j, T_{stg}$		-55 ... +175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
<b>Thermal characteristics<sup>2)</sup></b>						
Thermal resistance, junction - case	$R_{thJC}$		-	-	1.1	K/W
SMD version, device on PCB	$R_{thJA}$	minimal footprint	-	-	62	
		6 cm <sup>2</sup> cooling area <sup>4)</sup>	-	-	40	

**Electrical characteristics, at  $T_j=25\text{ °C}$ , unless otherwise specified**

#### Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	55	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=80\text{ }\mu\text{A}$	2.1	3.0	4	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=55\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.01	1	$\mu\text{A}$
		$V_{DS}=55\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}^{2)}$	-	1	100	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=50\text{ A}$	-	6.2	6.9	m $\Omega$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics<sup>2)</sup>**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	7800	8970	pF
Output capacitance	$C_{oss}$		-	1180	1770	
Reverse transfer capacitance	$C_{rss}$		-	1130	1700	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=27.5\text{ V},$ $V_{GS}=10\text{ V}, I_D=50\text{ A},$ $R_G=7\ \Omega$	-	30	-	ns
Rise time	$t_r$		-	60	-	
Turn-off delay time	$t_{d(off)}$		-	45	-	
Fall time	$t_f$		-	73	-	

**Gate Charge Characteristics<sup>2)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=11\text{ V}, I_D=50\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	46	61	nC
Gate to drain charge	$Q_{gd}$		-	28	43	
Gate charge total	$Q_g$		-	110	125	
Gate plateau voltage	$V_{plateau}$		-	5.9	-	V

**Reverse Diode**

Diode continuous forward current <sup>2)</sup>	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	50	A
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$		-	-	200	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=50\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	0.6	0.9	1.3	V
Reverse recovery time <sup>2)</sup>	$t_{rr}$	$V_R=27.5\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	45	-	ns
Reverse recovery charge <sup>2)</sup>	$Q_{rr}$		-	66	-	nC

<sup>1)</sup> Current is limited by bondwire; with an  $R_{thJC} = 1.1\text{ K/W}$  the chip is able to carry 104 A at 25°C. For detailed information see Application Note ANPS071E.

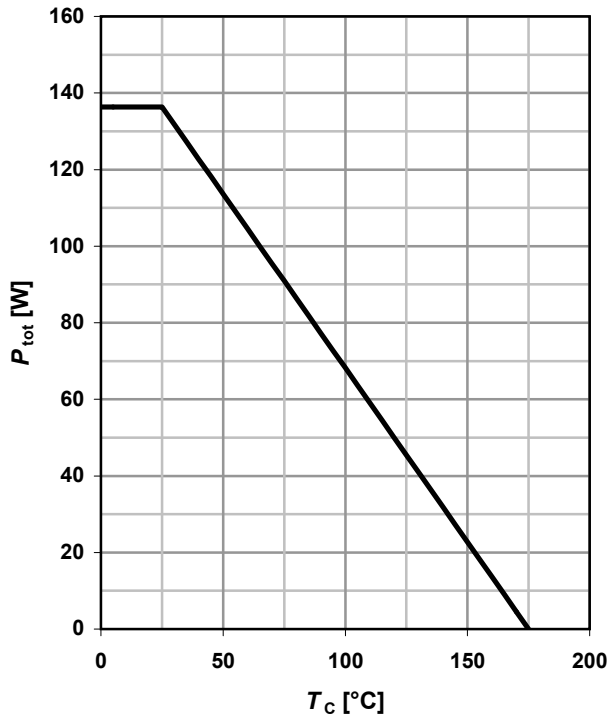
<sup>2)</sup> Defined by design. Not subject to production test.

<sup>3)</sup> Qualified at -5V and +20V.

<sup>4)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

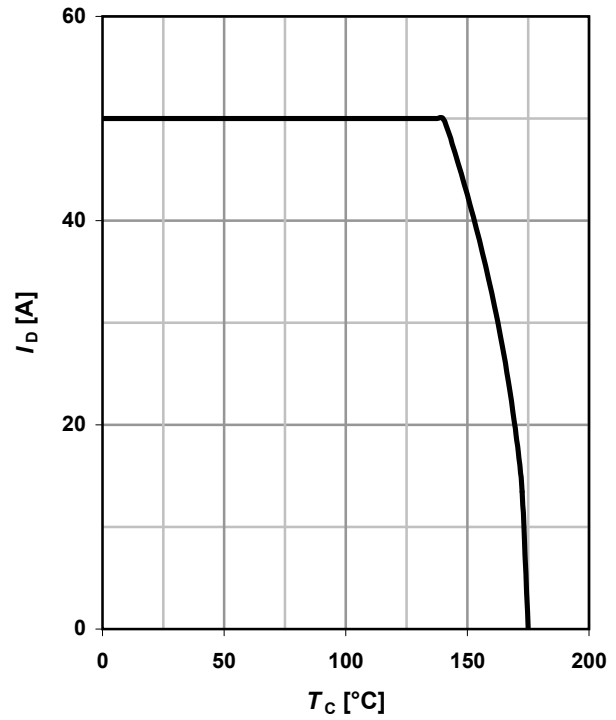
### 1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



### 2 Drain current

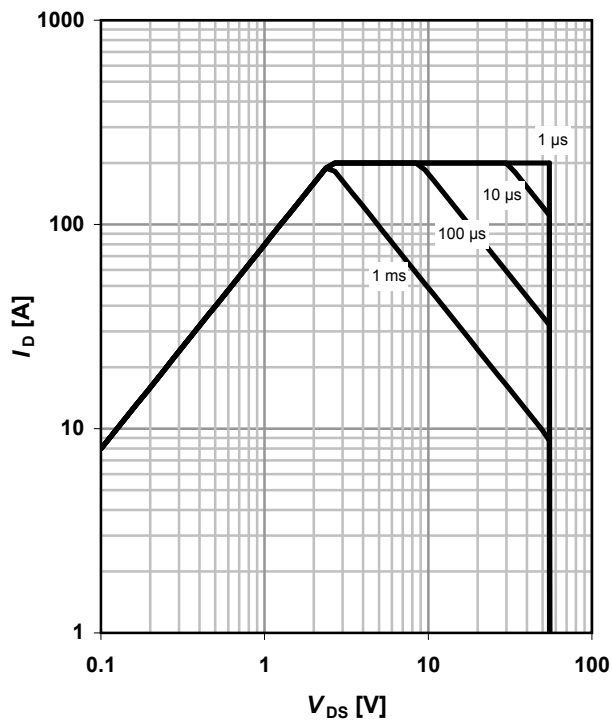
$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



### 3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

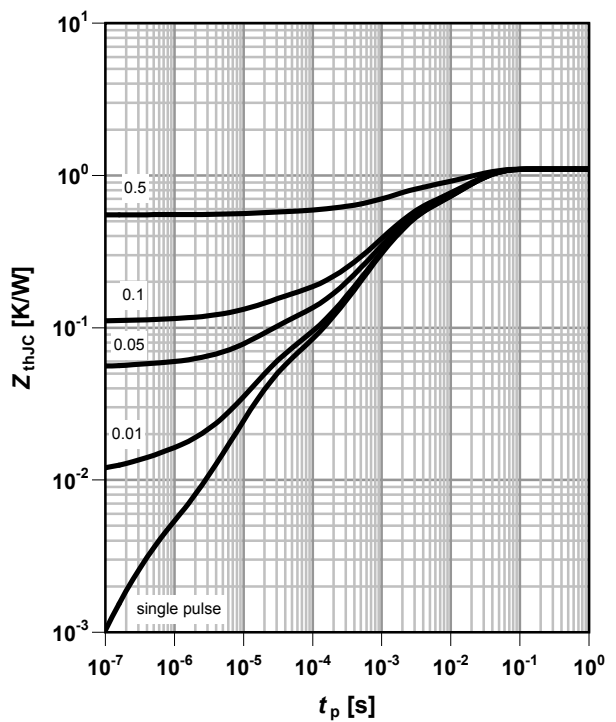
parameter:  $t_p$



### 4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

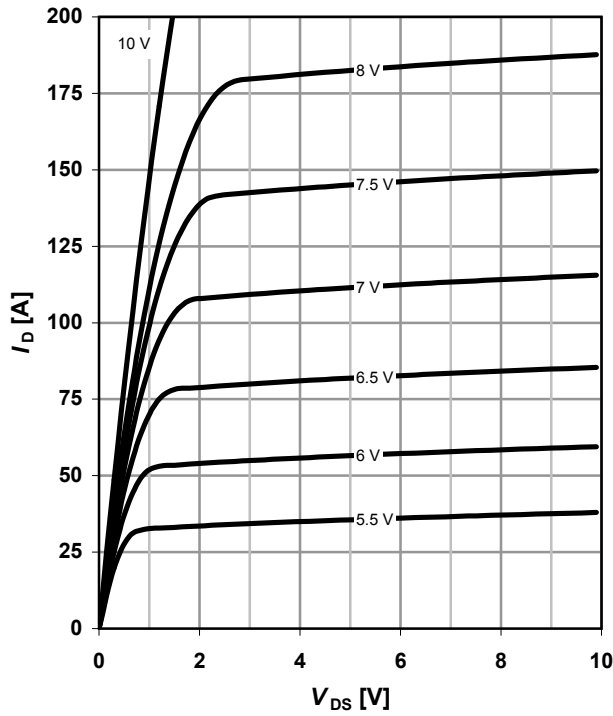
parameter:  $D = t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

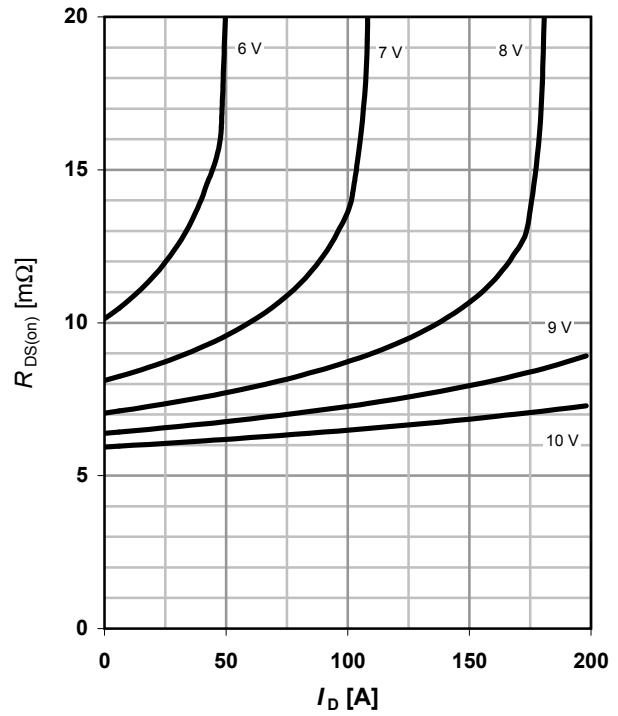
parameter:  $V_{GS}$



**6 Typ. drain-source on-state resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

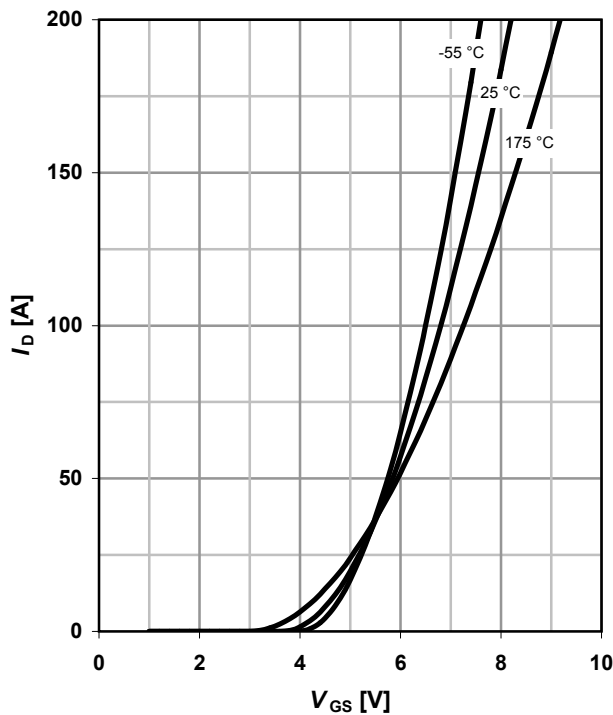
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

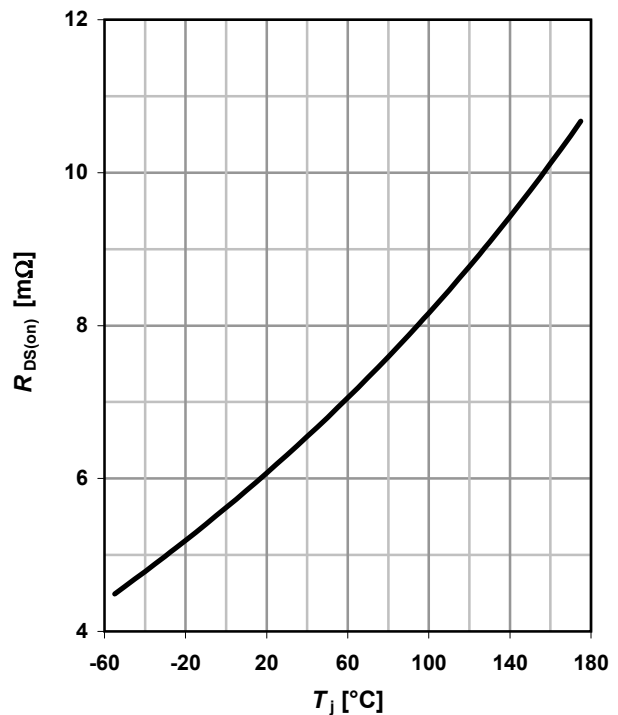
$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

parameter:  $T_j$



**8 Typ. drain-source on-state resistance**

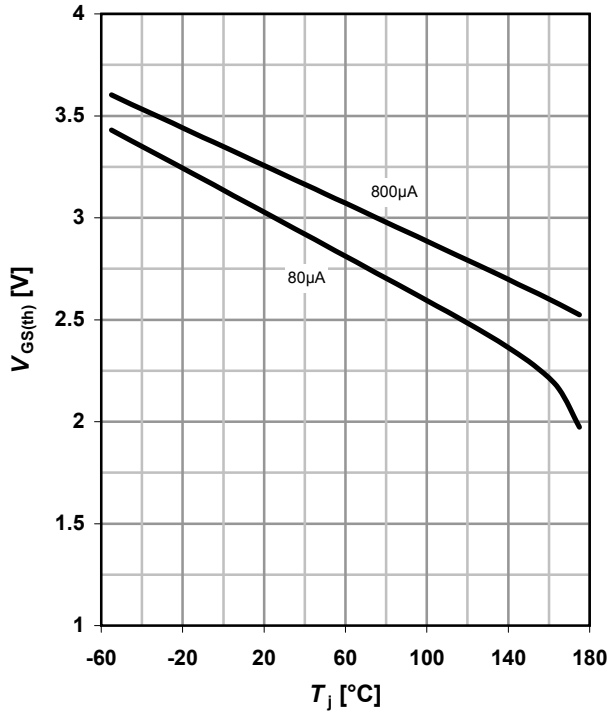
$R_{DS(on)} = f(T_j); I_D = 50\text{ A}; V_{GS} = 10\text{ V}$



**9 Typ. gate threshold voltage**

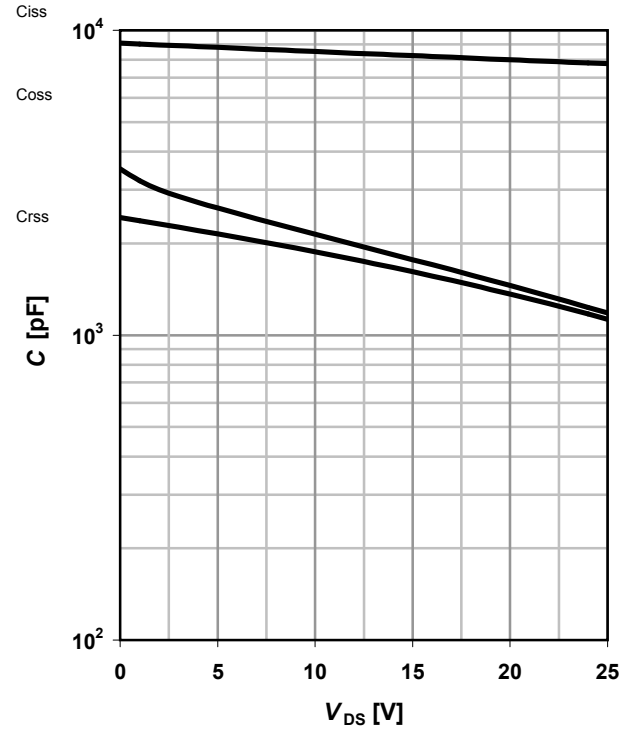
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter:  $I_D$



**10 Typ. capacitances**

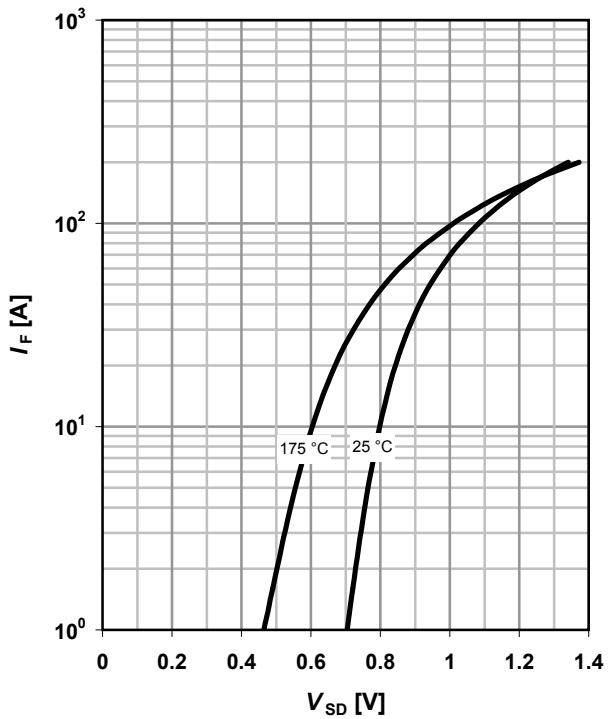
$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$



**11 Typical forward diode characteristics**

$I_F = f(V_{SD})$

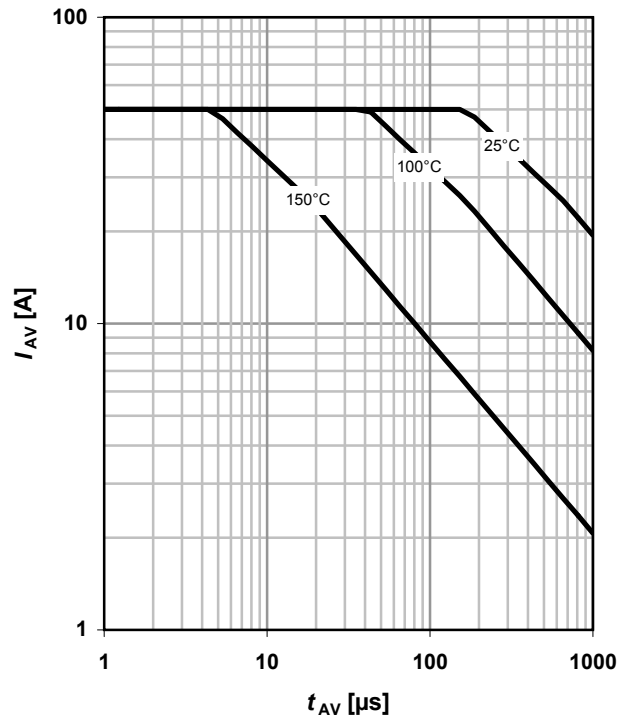
parameter:  $T_j$



**12 Typ. avalanche characteristics**

$I_{AV} = f(t_{AV})$

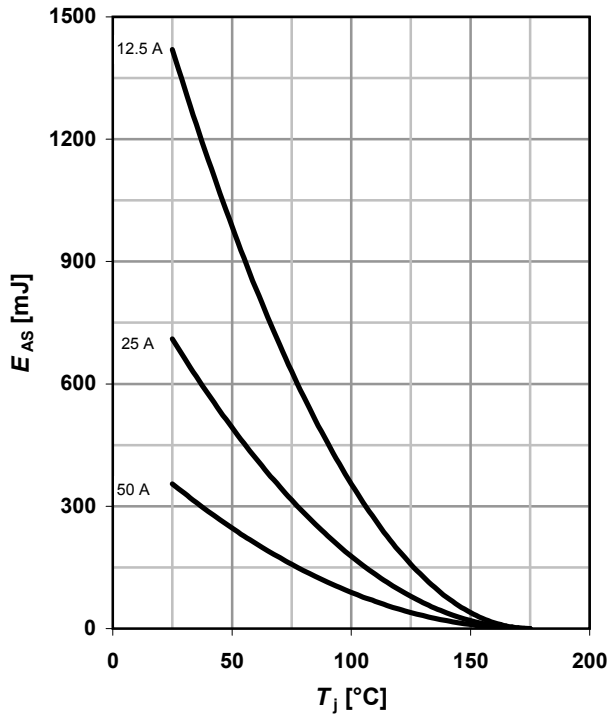
parameter:  $T_{j(start)}$



**13 Typical avalanche Energy**

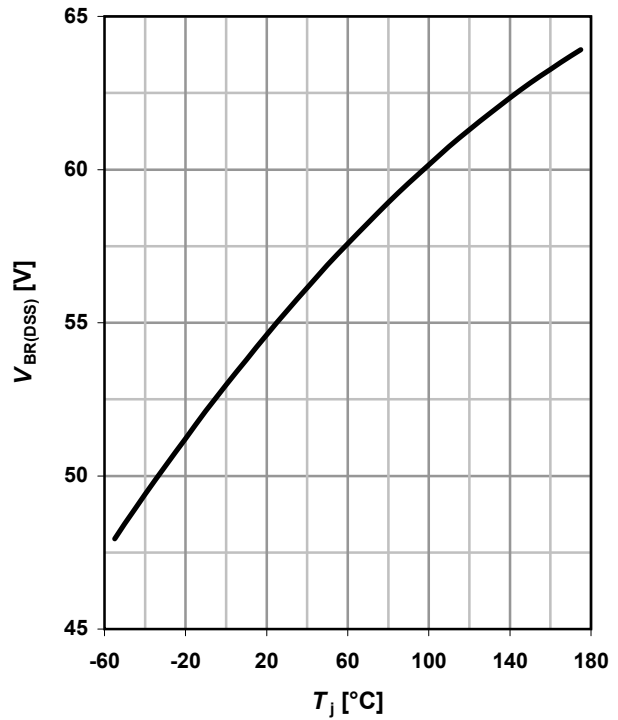
$E_{AS} = f(T_j)$

parameter:  $I_D$



**14 Drain-source breakdown voltage**

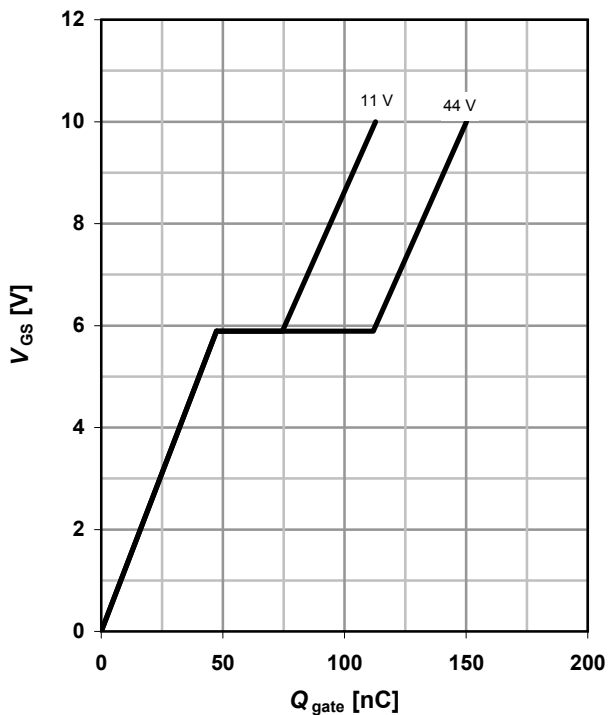
$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$



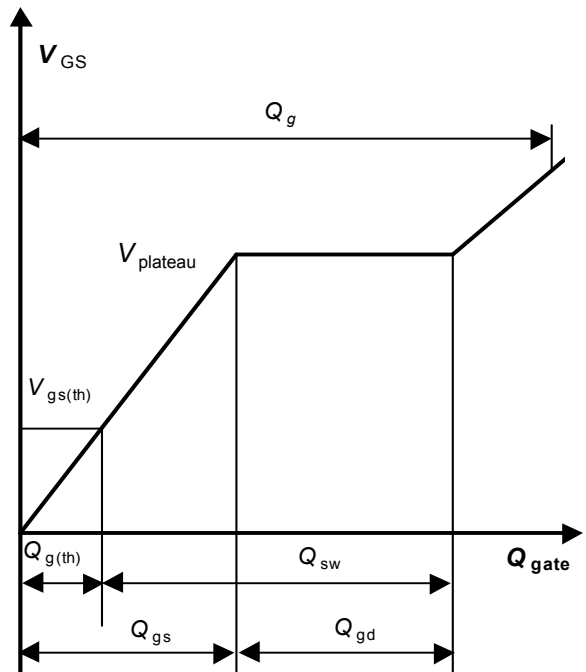
**15 Typ. gate charge**

$V_{GS} = f(Q_{gate}); I_D = 50 \text{ A pulsed}$

parameter:  $V_{DD}$



**16 Gate charge waveforms**



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## Revision History

Version	Date	Changes
Data Sheet version 1.1	07.11.2007	Implementation of avalanche current single pulse
Data Sheet version 1.1	07.11.2007	Update of package drawing
Data Sheet version 1.1	07.11.2007	Update of avalanche diagram 12 and 13
Data Sheet version 1.1	07.11.2007	implementation of footnote 2 for Eas specification